REMARKS

In response to the Final Office Action mailed June 6, 2005, Applicants respectfully request reconsideration.

Claims 1-8 have been examined. By this amendment, Applicants amend claims 1-5 and 8 for clarification. As a result, claims 1-8 are pending for examination, claims 1, 5, 7 and 8 being independent.

1. Claims 1-4 Patentably Distinguish Over Hadjiyiannis

Claim 1 stands rejected under §102(b) as purportedly being clearly anticipated by "ISDL: an instruction set description language for retargetability by Hadjiyiannis et al. (Hadjiyiannis). Applicants respectively traverse this rejection.

Hadjiyiannis is directed to using an instruction set description language (ISDL) to generate machine code from source code. (Abstract, page 299, second column, first full paragraph; page 300, first column, penultimate paragraph). A retargetable compiler receives source code and generates assembly code using the ISDL. (Fig. 1; page 300, first column, penultimate paragraph). The ISDL is also used to automatically generate an assembler, and the assembler transforms the assembly code to a binary file that is used as input to an Instruction Level Simulator (ILS). (Abstract; page 300, first column, an ultimate? paragraph).

Claim 1 has been amended as shown above solely for clarification. This amendment is support throughout the specification such as, for example, Fig. 2 and page 9, lines 4-18.

Claim 1 as amended patentably distinguishes over Hadjiyiannis because Hadjiyiannis does not disclose or suggest an assembler for a target microprocessor, the assembler comprising, *inter alia*, a descriptor file containing information descriptive of the instruction set of said target microprocessor. Rather, as discussed above, the ISDL description of Hadjiyiannis is used to automatically generate the assembler, but is not included within the assembler itself. Nor does Hadjiyiannis disclose or suggest that the automatically generated assembler makes any use of the ISDL description when generating binary files from assembly code.

In view of the forgoing, claim 1 patentably distinguishes over Hadjiyiannis. Accordingly, Applicants respectfully request that the rejection of claim 1 under §102(b) as being

anticipated by Hadjiyiannis be withdrawn. Claims 2-4 each depend from claim 1 and are patentable for at least the same reasons. Accordingly, Applicants respectfully request that the rejection of these claims be withdrawn.

2. Claims 5 and 6 Patentably Distinguish Over Hadjiyiannis

Claim 5 stands rejected under §102(b) as purportedly being clearly anticipated by Hadjiyiannis. Applicants respectfully traverse this rejection.

Claim 5 has been amended shown above solely for clarification. Claim 5 as amended patentably distinguishes over Hadjiyiannis because Hadjiyiannis does not disclose or suggest a method of assembling a machine language program for a target microprocessor comprising, *inter alia*, providing a descriptor file containing information descriptive of the instruction set of said target microprocessor, and **translating *assembly* language instructions into *machine* language wherein the translation comprises acquiring data from said descriptor file.** Rather, the automatically generated assembler of Hadjiyiannis does not acquire data from the ISDL description when it generates a binary file from assembly code. It is the compiler of Hadjiyiannis that uses the ISDL description to generate *assembly code* from *source code*.

In view of the foregoing, claim 5 patentably distinguishes over Hadjiyiannis. Accordingly, Applicants respectfully request that the rejection of claim 5 under §102(b) be withdrawn. Claim 6 depends from claim 5 and patentably distinguishes over the art of record for at least the same reasons. Accordingly, Applicants respectfully request that the rejection of claim 6 under §102(b) be withdrawn.

3. Claim 7 Patentably Distinguishes Over Hadjiyiannis in View of Vos

Claim 7 stands rejected under §103(a) as purportedly being unpatentable over Hadjiyiannis and further in view of GB 2, 127, 188 A (Vos). Applicants respectfully traverse this rejection.

Vos is directed to a system for translating hardware/software interface specifications simultaneously into specific microprocessor executable code and commands for the linker/loading system of a selected hardware configuration (page 1, lines 5-9). Contrary to the assertions of the Office Action (Sections 8 and 10), Vos does not teach a data capture device for

accessing *the instruction set* of said target microprocessor and having an output, wherein said output comprises a descriptor file containing information descriptive of said instruction set. The passages of Vos relied upon in the Office Action (page 2, lines 8-14) make no mention of an instruction set of a target processor, nor is this shown by the system components of Fig. 1 specified in the Office Action (i.e., interface requirements 2, prompter or editor 4, integration source file 6).

Even if the combination of Hadjiyiannis and Vos were proper (which it is not), claim 1 would patentably distinguish over such combination. Applicant notes preliminarily that claim 7 is not merely "a method version of . . . claims 1, 2 and 3" as characterized in the Office Action, but recites subject matter that is independently patentable from that of claims 1-3. Further, claim 7 patentably distinguishes over the combination of Hadjiyiannis and Vos because such combination does not teach or suggest a method of preparing a program executable on a target microprocessor comprising, *inter alia* capturing data from **the instruction set of said target microprocessor** thereby forming a descriptor file containing **information descriptive of said instruction set**, as recited in claim 7. As conceded in the Office Action, Hadjiyiannis does not disclose this limitation of claim 7. Further, as discussed above, Vos fails to remedy this deficiency as Vos is silent regarding the use of an instruction set of a said target microprocessor to form a descriptor file containing information descriptive of said instruction set. Accordingly, even if Hadjiyiannis and Vos were combined, no resulting combination of these references would employ a method comprising capturing data from an instruction set of a target microprocessor thereby forming a descriptive file containing information descriptive of said instruction set, as required by claim 7.

In view of the foregoing, claim 7 patentably distinguishes over Hadjiyiannis in view of Vos. Accordingly, Applicants respectfully request that the rejection of claim 7 under §103(a) be withdrawn.

4. <u>Claim 8 Patentably Distinguishes Over Hadjiyiannis in View of Vos</u>

Claim 8 stands rejected under §103(a) as purportedly being unpatentable over Hadjiyiannis and further in view of Vos. Applicants respectfully traverses this rejection.

Claim 8 has been amended as shown above solely for clarification. Claim 8 patentably distinguishes over Hadjiyiannis in view of Vos because such combination does not teach or suggest a method of preparing a program executable on a microprocessor, comprising, *inter alia*, providing a descriptor file containing information descriptive of the instruction set of said target microprocessor, and **translating *assembly* language instructions into *machine* language wherein the translation comprises acquiring data from said descriptor file**, as recited in claim 8. As discussed above, Hadjiyiannis does not disclose or suggest acquiring data from a descriptor file as part of translating assembly language instructions into machine language. There is simply no teaching in Hadjiyiannis that the automatically generated assembler acquires data from the ISDL description. Rather, it is the compiler that uses that the ISDL description to generate *assembly code* from *source code*. Further, Vos fails to remedy the deficiencies of Hadjiyiannis. Accordingly, even if it were proper to combine Hadjiyiannis and Vos (which it is not), no resulting combination of these references would employ a method comprising translating assembly language instructions into machine language wherein a translation step comprises acquiring data from a descriptor file containing information descriptive of the instruction set of said target microprocessor, as required by claim 8.

In view of the foregoing, claim 8 patentably distinguishes over the combination of Hadjiyiannis and Vos. Accordingly, Applicants respectfully request that the rejection of claim 8 under §103(a) be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 1, 2005.

Janine Michalski

Attorney Docket No.: S1022.80572US00
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Respectfully submitted,

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